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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/541,957	02/02/2006	Walter Fix	411000-138	8170
27162 7590 05/17/2007 CARELLA, BYRNE, BAIN, GILFILLAN, CECCHI, STEWART & OLSTEIN 5 BECKER FARM ROAD ROSELAND, NJ 07068			EXAMINER CHHAYA, SWAPNEEL	
			ART UNIT 2822	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	Application No. 10/541,957	Applicant(s) FIX ET AL.	
	Examiner Swapneel Chhaya	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 08 July 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 July 2005 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>07/08/2005 and 11/04/2005</u> . | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the semiconducting layer and insulating layer of claim 1 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to under 37 CFR 1.83(a) because they fail to show figure 1a and through-contact 10b as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "3" and "13" have both been used to designate the gate

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and/or channel. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Claim Objections***

4. Claim 20 objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 20 depends on claim 17 and it is the same claim as claim 17.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 2, 5, 6, 9, 10, 14, 17, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Hart U.S. Patent (6, 362, 509).

Regarding claim 1, An organic field effect transistor (10, 20, Fig. 1) including a gate (18, 28, Fig.1) comprising:

at least

a first electrode layer forming a source or a drain electrode (14, 15, Fig. 2a, column 5 lines 15-30, 47-55) and having multiple sides

a semiconducting layer (5, Fig. 1, column 5 lines 15-30)

an insulator layer (6, Fig. 1, column 5 lines 15-30); and

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a second electrode layer forming the other of said source and drain electrodes (14, 15, Fig. 2a, column 5 lines 15-30, 47-55) and having multiple sides wherein the source or drain electrode in the first electrode layer surrounds the respective other electrode of the second electrode layer in a two-dimensional manner with the exception of one of said sides of the other electrode

whereby a u-shaped and/or meandering current channel (Fig. 2a), which begins and ends on one of said sides of the electrode of the first electrode layer, is formed in the semiconducting layer, please note that the examiner is referring to the area between the two electrodes.

Regarding claim 2, The OFET as claimed in claim 1 wherein, in the first electrodes layer respectively bounds the other electrode layer on three of four sides (Fig.2a)

Regarding claim 5 and 14, An integrated circuit having at least two OFETs (10, 20, 30) as claimed in claim 1 wherein the at least two OFETs are arranged into a NAND (51) or NOR gate such that the one sides of the two OFETs are respectively opposite one another.(Fig. 2 column 5 lines 46-60)

Regarding claim 6, 17, and 20, the integrated circuit as claimed in claim 5; including

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connecting lines (39) and/or inputs (19, 29) and outputs respectively situated in a region between the one sides.(Fig. 2 column 5 lines 50-65)

Regarding claim 9, the integrated circuit as claimed in claim 5 including a through-contact (42) in said first electrode layer (Fig. 2a column 5 lines 50-60)

Regarding claim 10 The integrated circuit as claimed in claim 9, wherein the through-contact (42) extends at least to one further side of the OFET other than said one side (Fig. 2a column 5 lines 50-60)

### ***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 3, 11, 15, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hart (U.S. Patent 6, 362, 509).



Regarding claims 3 and 11, The OFET as claimed in claim 1 wherein the second electrode layer (14, 24, 34) completely covers the current channel of the first electrode layer (15, 25) and, in addition, at least one other part of the first electrode layer (15, 25, 35) (Fig. 2A column 5 lines 46-60)

Hart discloses the claimed invention in claims 3 and 11 except for the additionally covered part having a width in the range from 0 to 20  $\mu\text{m}$  and having a length in the range of the length of the current channel.. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the range from 0 to 20  $\mu\text{m}$ , since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

Regarding claim 15, Hart discloses an integrated circuit having at least two OFETs (10, 20, 30) as claimed in claim 3 wherein the at least two OFETs are arranged into a NAND (51) or NOR gate such that the one sides of the two OFETs are respectively opposite one another. (Fig. 2 column 5 lines 46-60)

Regarding claim 18, the integrated circuit as claimed in claim 15; including connecting lines (39) and/or inputs 19, 29) and outputs respectively situated in a region between the one sides. (Fig. 2a column 5 lines 50-65).

9. Claims 4, 7, 8, 12, 13, 16, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hart as applied to claims 1 and 3 above in view of Ahn et Al. (U.S. Patent 6, 559, 920).

Regarding claims 4, 7, 8, 12 and 13, Hart discloses the claimed invention except for the holes and/or interruptions present in the semiconductor layer and/or between the one sides. Ahn teaches that it is known to have holes and/or interruptions are in the semiconductor layer (202, Fig. 5B, 5D column 5 lines 9-11). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate holes and/or interruptions as taught by Ahn, since Ahn states at column 5 lines 10-11 that such a modification would decrease leakage current.

Regarding claim 16, Hart discloses an integrated circuit having at least two OFETs (10, 20, 30) as claimed in claim 4 wherein the at least two OFETs are arranged into a NAND (51) or NOR gate such that the one sides of the two OFETs are respectively opposite one another. (Fig. 2A column 5 lines 46-60)

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Regarding claim 19, Hart discloses the integrated circuit as claimed in claim 5; including connecting lines (39) and/or inputs (19, 29) and outputs respectively situated in a region between the one sides.(Fig. 2a column 5 lines 50-65)

### ***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Deeleuv et. Al. (U.S. Patent 6, 818, 920) discloses an invention of note.

Amundson et Al. (U.S. Patent 6, 545, 291) discloses an invention of note.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Swapneel Chhaya whose telephone number is 571-270-1434. The examiner can normally be reached on Monday- Thursday 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SC

  
Zandra V. Smith  
Supervisory Patent Examiner  
14 May 2007